UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/501,845 | 08/26/2005 | Martin Vorbach | 2885/86 | 9148 |

26646 7590 11/19/2008

KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

| EXAMINER | |
|---|---|
| VICARY, KEITH E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 11/19/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/501,845 | VORBACH ET AL. | |
| | Examiner | Art Unit | |
| | Keith Vicary | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *7-13,15-17 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13,15-17 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/19/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 7-13, 15-17, and 19-22 are pending in this examination and presented for examination. Claim 7 is currently amended and claims 19-22 are added by an amendment filed 8/19/2008.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 7-13, 15-17, and 19-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Given the quantity of further disclosures that have been incorporated by reference, any subject matter which is described only in separate disclosures and which would overcome the written description issues described below should have their locations explicitly cited in applicant remarks. Applicant is reminded that applicant is required to amend the disclosure to include the material incorporated by reference, if the material is relied upon to overcome any objection, rejection, or other requirement imposed by the Office.

5. Claim 7 recites the limitation "wherein the register has a data stream memory designed as a vector memory" in lines 2-3. However, the original disclosure does not appear to disclose how a register which has a data stream memory is *designed* as a vector memory.

6. Claim 7 recites the limitation "each of the configurations is handled as a single instruction" in lines 10. While the original disclosure does disclose of a traditional instruction being replaced by a CIW, the original disclosure does not appear to disclose what it means for a configuration to be *handled* as a single instruction.

a. Claims 8-13, 15-17, and 19-22 are rejected for failing to alleviate the rejection of claim 7 above.

7. Claim 19 recites the limitation "the handling of the configurations as the single instructions is directly by an operating system." The original disclosure does not appear to disclose that the handling of the configurations as the single instructions is directly by an operating system.

8. Claim 22 recites the limitation "the system trap is handled by an operating system as an illegal instruction" in lines 1-2. The original disclosure does not appear to disclose of system traps due to watchdog signals being associated with illegal instructions, as opposed to an invalid instructions.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 7-13, 15-17, and 19-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 7 recites the limitation "wherein the register has a data stream memory designed as a vector memory" in lines 2-3. It is indefinite as to how a register which has a data stream memory can be "designed" as a vector memory. In other words, it is unclear as to how a memory can be "designed" as a vector memory, as opposed to just containing vector data thereon.

12. Claim 7 recites the limitation "each of the configurations is handled as a single instruction" in lines 10. It is indefinite as to what is meant by the "handled" limitation. For example, this limitation could mean that a configuration goes through a general purpose microprocessor the same way as a regular software instruction, or a configuration is handled as a single instruction in that causes only one configuration of the data processing cells per configuration and not multiple configurations of the data processing cells, or a configuration is replaced by a single instruction such that the single instruction performs the configuration function.

b. Claims 8-13, 15-17, and 19-22 are rejected for failing to alleviate the rejection of claim 7 above.

13. Claim 19 recites the limitation "the handling of the configurations as the single instructions is directly by an operating system." It is indefinite as to what is meant by this limitation. For example, it is indefinite as to whether the association of the configuration with a single instruction is done by the operating system, or whether the

execution of the configuration is done by the operating system, or so forth. It is indefinite as to whether the handling is *done* directly by an operating system, or whether the handling takes place at a location or environment directly by (near) an operating system.

14. Claim 21 recites the limitation "the watchdog signal" in line 1. There is insufficient antecedent basis for this limitation in the claim.

c. Claim 22 is rejected for failing to alleviate the rejection of claim 21 above.

15. Claim 22 recites the limitation "the system trap is handled by an operating system as an illegal instruction" in lines 1-2. It is indefinite as to what is meant by the limitation "handled." It is further indefinite as to how a system trap can be handled as an illegal instruction, as a system trap is usually initiated in response to an illegal instruction and is not an illegal instruction itself. It is indefinite as to whether the use of "illegal instruction" is referring to an invalid instruction in general, or an instruction with an illegal opcode.

### *Claim Rejections - 35 USC § 103*

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 7-10, 15-17, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (Smith) (US 6658564 B1) in view of Panwar et al. (US PAT 5941977) in view of Gee et al. (Gee) (US 6374286).

18. Consider claim 7, Smith discloses providing a program corresponding to a sequence of compilable high-level language instructions (col. 10, lines 49-50, high-level design specification or algorithm); determining, for the reconfigurable field of data processing cells (col. 8, lines 52-53, programmable logic resources), a set of configurations by execution of which the program is run (col. 11, lines 60-63, compiling hardware functions into configuration patterns using a hardware description language compiler), wherein each of the configurations is handled as a single instruction (for example, col. 10, lines 1-6, discloses that functions may be used for rendering surfaces or for ray tracing, thus a configuration can be logically thought of as an instruction which performs surface rendering or ray tracing. As another example, there is no requirement that a function must be a certain amount of instructions; a configuration can perform the function of a single instruction); executing the configurations (col. 10, lines 50-51, executing on a reconfigurable hardware architecture); and during the executing: storing, in the data stream memory, at least one of the data stream and parts of the data stream (col. 4, lines 22-33, disclose of the random-access memory devices, it is inherent may be written to), where the data stream memory is designed as a vector memory (it is inherent that a data stream memory holds vectors of bits, such as each addressable line).

However, Smith does not explicitly disclose that the data stream memory is a register. Smith also does not disclose determining, for each configuration, a respective maximum allowed execution runtime prior to lapse of which the respective configuration is uninterruptible, and for each configuration, monitoring the respective maximum allowed execution runtime in order to interrupt the configuration if the respective maximum allowed execution runtime is exceeded.

On the other hand, Panwar does disclose a register (col. 2, lines 26-29 and col. 7, line 31, registers).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that one of many motivations of having a register act as a memory would be to allow quick access to data.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Panwar with the invention of Smith in order to allow quicker access to the data stream.

However, neither Smith nor Panwar disclose determining, for each configuration, a respective maximum allowed execution runtime prior to lapse of which the respective configuration is uninterruptible, and for each configuration, monitoring the respective maximum allowed execution runtime in order to interrupt the configuration if the respective maximum allowed execution runtime is exceeded.

On the other hand, Gee does disclose of determining, for each context, a respective maximum allowed execution runtime prior to lapse of which a respective partition is uninterruptible, and for each partition, monitoring the respective maximum

allowed execution runtime in order to interrupt the configuration if the respective maximum allowed execution runtime is exceeded (see, for example, col. 28, lines 37-44, watchdog timers which enforce context switches between the various partitions, configurable time-out limits, or col. 23, lines 56-64, the time duration of the partitions can be of different lengths; col. 28, line 45-51, interrupt).

Gee's teaching of his watchdog timer enforces context switches between the various applications to ensure partition scheduling is performed and the processor is kept running in the event of a software error (Gee, col. 28, lines 37-44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Gee with the invention of Smith and Panwar in order to ensure partition scheduling is performed and the processor is kept running in the event of a software error.

19. Consider claim 8, Panwar does disclose at least one: I) of a register allocation device to allocate the register, and ii) a register releasing device to release the register (col. 7, lines 31-39, register window allocation and 54-64, register management).

20. Consider claim 9, Panwar discloses that the register allocation device is preserved over multiple reconfigurations of the reconfigurable field of data processing cells (col. 2, lines 25-42, col. 6, lines 32-36, col. 7, lines 31-39 and 54-64; the multithreading aspect in which each thread has its corresponding registers conserved correlates to the different reconfigurations).

21. Consider claim 10, Smith discloses that the register is a RAM PAE (col. 4, lines 22-33, disclose of the random-access memory devices).

22. Consider claim 15, Gee discloses a watchdog is used to recognize an exceedance of each respective maximum allowed execution runtime (see, for example, col. 28, lines 37-44, watchdog timers which enforce context switches between the various partitions, configurable time-out limits, or col. 23, lines 56-64, the time duration of the partitions can be of different lengths; col. 28, line 45-51, interrupt).

23. Consider claim 16, Gee discloses that any one of the configurations that exceeds its respective maximum allowed execution runtime is treated as illegal (see, for example, col. 28, lines 37-44, watchdog timers which enforce context switches between the various partitions, configurable time-out limits, or col. 23, lines 56-64, the time duration of the partitions can be of different lengths; col. 28, line 45-51, interrupt).

24. Consider claim 17, Gee discloses that any one of the configurations that exceeds its respective maximum allowed execution runtime is treated as illegal (see, for example, col. 28, lines 37-44, watchdog timers which enforce context switches between the various partitions, configurable time-out limits, or col. 23, lines 56-64, the time duration of the partitions can be of different lengths; col. 28, line 45-51, interrupt).

25. Consider claim 19, Smith discloses the handling of the configurations as the single instructions is directly by an operating system (col. 12, lines 5-8, functions are inputs to the VCOS).

26. Consider claim 20, Smith discloses at least one of the configurations calls another of the configurations as a sub-routine (col. 12, lines 1-5 for example, a main function calls a dynamically-linked function).

27. Consider claim 21, Gee discloses the watchdog signal initiates a system trap (col. 28, line 49, discloses of an interrupt, a trap can be defined as a program interrupt).

28. Consider claim 22, Gee discloses the system trap is handled by an operating system as an illegal instruction (an operating system takes appropriate action in response to a watchdog signal just as it would take appropriate action in response to an illegal instruction).

29. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, Panwar, and Gee as applied to claim 7 above, and further in view of Dockser (US PAT 5860119).

30. Consider claim 11, Panwar discloses a register (col. 2, lines 26-29 and col. 7, line 31 as above) and both Smith and Gee discloses of multitasking and executing of at least one of two different tasks of the multitask application (Smith, col. 9, lines 1-4,

multitasking; Gee, col. 28, lines 37-44 as above, context switching). However, Smith, Panwar, and Gee do not explicitly disclose the register configured to provide read and write access when a virtual FIFO dividing line is implemented.

On the other hand, Dockser does disclose register configured to provide read and write access (col. 4, lines 32-35, receive mode and transmit mode, and col. 5, lines 56-65, read and write pointers) when a virtual FIFO dividing line is implemented (col. 3, lines 10-30, lines 54-56; the last word flag and end-of-packet detection means correlate to the said virtual FIFO dividing line).

Using the invention of Dockser in general makes a FIFO system both simple and inexpensive to implement (Dockser, col. 4, lines 6-40), despite decreases in management overhead.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the FIFO modifications taught by Dockser with the invention of Smith, Panwar, and Gee in order to implement the FIFO simply and inexpensively while simultaneously minimizing management overhead.

31. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, Panwar, and Gee as applied to claim 7 above, and further in view of Davis et al. (Davis) (US PAT 4041462).

32. Consider claim 12, Smith, Panwar, and Gee do not explicitly disclose at least one memory unit configured for use as a stack and being configured to indicate at least one of a stack underflow state and a stack overflow state.

On the other hand, Davis does disclose at least one memory unit configured for use as a stack and being configured to indicate at least one of a stack underflow state and a stack overflow state (col. 14, lines 1-4, limit checking facilities which test for overflow and underflow, and lines 21-32, PSW)

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that stacks in general are an easily implemented method of dynamic allocation of storage space for data, and a simple efficient mechanism for enqueuing data and/or parameters.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the stacks of Davis with the invention of Smith, Panwar, and Gee in order to easily implement a method of dynamic allocation of storage space for data, and efficiently enqueue data and/or parameters.

33. Consider claim 13, the claim is rejected for the same reasons as claim 12 above. In addition, Davis discloses the at least one measuring unit is configured to indicate the at least one of the underflow state and overflow state of an operating system unit (col. 14, lines 1-4 and lines 21-32; also, note the PSW is typically accessed by the operating system).

***Response to Arguments***

34. Applicant argues on page 6 that claim 7 now recites that data stream memory is one "designed as a vector memory" whereas Smith merely refers to RAM devices.

However, this Smith nevertheless teaches the limitation when interpreted broadly, as explained above. In addition, the limitation is indefinite, and is also located in the preamble.

35. Applicant argues on page 6 that Gee's teaching is directed toward JVMs and not configurations. However, the general concept of not allowing a slice of processing to indefinitely run and maintain control of resources is applicable regardless of whether the slice of processing is a JVM executing a number of applications or threads of Gee, of the configurations of Smith.

36. Applicant argues on the bottom of page 6 that neither of the cited references suggest such an application or indicate how such an application may be implemented. However, the examiner has described how the prior art teaches the claimed limitations with the appropriate motivations.

37. Applicant argues on page 7 that the configurations of Smith are classical configurations which are not handled as instructions, whereas the amended claim provides that each of the configurations is handled as a single instruction. However, the limitation wherein a configuration is "handled" as a single instruction can be broadly interpreted as done in the rejection above. Applicant does elaborate on examples as to what a configuration of Smith does not include; however, these examples do not elucidate what is meant by the limitation "handling." For example, it is argued that a

configuration of Smith is not handled by an operating system, though Smith discloses how configurations are inputs to the virtual computer operating system in col. 12, lines 1-8. Moreover, even if these examples were to more narrowly define what is meant for a configuration to be "handled" as an instruction, the concepts behinds these examples are not claimed.

38. Applicant argues on page 7 that defining a maximum run time for a configuration, where configurations correspond to instructions, would not have been thought of by the average skilled person. However, Gee teaches of defining maximum run times to keep a processor running in the event of a software error; this motivation is applicable whether the software error is due to a single instruction corresponding to a configuration or a single instruction of a group of instructions corresponding to a configuration. Applicant states a maximum run time for a configuration would not be necessary for an instruction in a "conventional" processor; however the behavior of a "conventional" processor appears to be moot as Smith as modified by Gee would still teach the claimed limitations. Applicant argues that, given the combination, the average skilled person would still not end up in a more favorable situation with regard to debugging. However, any considerations regarding debugging explicitly are not claimed. The claims may recite limitations which are added in order to support debugging (such as the data stream memory); however, there are no limitations relating the aforementioned limitations to the debugging process in particular and their relationship to restricting runtime.

39. Examiner recommends elaborating on what it means for a configuration to be "handled" as a single instruction or reciting limitations which explain the debugging procedure in order to overcome the current prior art.

***Conclusion***

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

d. Crosland et al. (US 7350178 and US 7340596) discloses of an embedded processor with watchdog timer for programmable logic.

e. Allen et al. (US 7000161) discloses of a reconfigurable programmable logic system with configuration recovery mode.

41. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 6:15 a.m. - 5:45 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/Keith Vicary/
Examiner, Art Unit 2183